## Claims

What is claimed is:

1. A system for testing an embedded electronic systems having a target processor executing a target program and coupled to target hardware that may be partially physical and partially simulated, the system comprising:

a hardware simulator configured to simulate the simulated portion of the target hardware;

a target monitor coupled to the target processor, the target monitor being operative to determine when the target processor is attempting to communicate with the simulated portion of the target hardware and to suspend execution of the target program in response thereto, the target monitor further being operative to convert output signals from the target processor that are directed to the simulated hardware to corresponding output data and to convert input data from the hardware simulator to corresponding input signals that are applied to the target processor; and

a communications interface coupling the target monitor to the hardware simulator, the communications interface being operative to transfer the output data from the target monitor to the hardware simulator and being operative to transfer the input data from the hardware simulator to the target monitor.

2. The system of claim 1 further comprising a microprocessor emulator containing the target processor and a memory device containing the target program.

3. The system of claim 1 wherein the target monitor comprises:

a mapping memory recording addresses in the address space of the simulated hardware; and

an address comparator coupled to the mapping memory and an address bus of the target processor, the address comparator comparing an address on the address bus to addresses recorded in the mapping memory and suspending execution

of the target program in response to a match between the address on the address bus and an addresses recorded in the mapping memory.

4. The system of claim 1 wherein the target monitor comprises:

a control signal monitor monitoring a terminal on the target processor that is adapted to receive a control signal from the physical hardware in the event of an access to the physical hardware by the target processor, the control signal monitor generating a detect signal in response to receiving the control signal; and

a timer coupled to the target processor and the control signal monitor, the timer initiating a timing period responsive to an access by the target processor to the target hardware and suspending execution of the target program after the timing period has been initiated unless the detect signal has been received within a predetermined period after initiating the timing period.

5. The system of claim 6 wherein the control signal comprises an acknowledge signal adapted to be generated by the physical hardware responsive to an access by the target processor to the physical hardware.

6. The system of claim 1 wherein the target monitor comprises:

a target processor bus driver circuit operative to receive the input signals from the control processor and to apply the input signals to the target processor; and

a target processor bus capture circuit operative to apply the output signals from the target processor to the control processor.

7. The system of claim 1 wherein the communications interface comprises an Ethernet link coupling the target monitor to the hardware simulator.

8. The system of claim 1 wherein the hardware simulator comprises a host computer programmed with a hardware simulation program that simulates the simulated portion of the target hardware.

9. The system of claim 8 further comprising a microprocessor emulator containing the target processor and a memory device containing the target program, the microprocessor emulator being coupled to the host computer to serve as a user interface for the emulator.

10. A system for testing an embedded electronic systems having a target processor adapted to execute a target program, the target processor being coupled to target hardware that may be partially physical and partially simulated, the system comprising:

a mapping memory recording addresses in the address space of the simulated hardware;

an address comparator coupled to the mapping memory and an address bus of the target processor, the address comparator comparing an address on the address bus to addresses recorded in the mapping memory and suspending execution of the target program in response to a match between the address on the address bus and an addresses recorded in the mapping memory;

a target processor bus capture circuit operative to store output signals from the target processor responsive to the address comparator detecting a match between the address on the address bus and an addresses recorded in the mapping memory;

a signal converter converting the output signals stored in the bus capture circuit operative to corresponding output data; and

a communications interface coupling the signal converter to the hardware simulator, the communications interface transferring the output data from the signal converter to the hardware simulator and coupling the input data from the hardware simulator to the target processor bus jammer circuit.

11. The system of claim 10 further comprising:

a second signal converter coupled to the hardware simulator, the second signal converter converting input data from the hardware simulator to corresponding input signals; and

a target processor bus driver circuit coupled to the second signal converter, target processor bus driver being operative to apply the input signals to the target processor.

12. The system of claim 10 further comprising a microprocessor emulator containing the target processor and a memory device containing the target program.

13. The system of claim 10 wherein the communications interface comprises an Ethernet link coupling the signal converter to the hardware simulator.

14. The system of claim 10 wherein the hardware simulator comprises a host computer programmed with a hardware simulation program that simulates the simulated portion of the target hardware.

15. The system of claim 14 further comprising a microprocessor emulator containing the target processor and a memory device containing the target program, the microprocessor emulator being coupled to the host computer to serve as a user interface for the emulator.

16. A system for testing an embedded electronic systems having a target processor adapted to execute a target program, the target processor being coupled to target hardware that may be partially physical and partially simulated, the system comprising:

a control signal monitor monitoring a terminal on the target processor that is adapted to receive a control signal from the physical hardware in the event of an access to the physical hardware by the target processor, the control signal monitor generating a detect signal in response to receiving the control signal; and

a timer coupled to the target processor and the control signal monitor, the timer initiating a timing period responsive to a hardware access by the target processor and suspending execution of the target program after the timing period has been initiated unless the detect signal has been received within a predetermined period after initiating the timing period;

a target processor bus capture circuit operative to store output signals from the target processor after the timing period has been initiated unless the detect signal has been received within a predetermined period after initiating the timing period;

a signal converter converting the output signals stored in the bus capture circuit operative to corresponding output data; and

a communications interface coupling the signal converter to the hardware simulator, the communications interface transferring the output data from the signal converter to the hardware simulator.

17. The system of claim 16 further comprising:

a second signal converter coupled to the hardware simulator, the second signal converter converting input data from the hardware simulator to corresponding input signals; and

a target processor bus driver circuit coupled to the second signal converter, target processor bus driver being operative to apply the input signals to the target processor.

18. The system of claim 16 further comprising a microprocessor emulator containing the target processor and a memory device containing the target program.

19. The system of claim 16 wherein the communications interface comprises an Ethernet link coupling the signal converter to the hardware simulator.

20. The system of claim 16 wherein the hardware simulator comprises a host computer programmed with a hardware simulation program that simulates the simulated portion of the target hardware.

21. The system of claim 20 further comprising a microprocessor emulator containing the target processor and a memory device containing the target program, the microprocessor emulator being coupled to the host computer to serve as a user interface for the emulator.

22. A method of testing an embedded electronic systems having a target processor adapted to execute a target program, the target processor being coupled to target hardware that may be partially physical and partially simulated, the method comprising

monitoring signals present on a plurality of externally accessible terminals of the target processor as the target processor executes the target program;

determining when the target processor is attempting to access the simulated portion of the target hardware on the basis of the monitored signals;

in response to determining that the target processor is attempting to access the simulated portion of the target hardware, suspending execution of the target program; and

in response to determining that the target processor is attempting to access the simulated portion of the target hardware, processing output signals present on a plurality of the externally accessible terminals in a hardware simulator.

23. The method of claim 22 further comprising:

determining when the target processor is attempting to access the physical portion of the target hardware on the basis of the monitored signals; and

in response to determining that the target processor is attempting to access the physical portion of the target hardware, allowing the target processor to access the physical portion of the target hardware.

24. The method of claim 22 further comprising:

receiving input data from the hardware simulator responsive to processing the output signals;

converting the input data to corresponding input signals; and

applying the input signals to the externally accessible terminals.

25. The method of claim 22 wherein the step of determining when the target processor is attempting to access the simulated portion of the target hardware comprises:

recording addresses that are in the address space of the simulated hardware;

comparing an address on the address bus of the target processor to the recorded addresses; and

detecting a match between the address on the address bus and a recorded address.

26. The method of claim 22 wherein the step of determining when the target processor is attempting to access the simulated portion of the target hardware comprises:

monitoring a terminal on the target processor that is adapted to receive a control signal from the physical hardware in the event of an access to the physical hardware by the target processor;

initiating a timing period responsive to a target hardware access by the target processor; and

detecting if the control signal is received from the physical target hardware within a predetermined period after initiating the timing period.

27. The method of claim 22 further comprising:

detecting an interrupt signal applied to the target processor during the time that the target processor has suspended execution of the target program; and

executing an interrupt routine responsive to the interrupt signal.

28. The method of claim 22 further comprising:

detecting data from the hardware simulator corresponding to an interrupt signal;

in response to detecting data from the hardware simulator corresponding to an interrupt signal, applying an interrupt signal to the target processor; and

in response to the interrupt signal, allowing the target processor to execute an interrupt routine.